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Controlling the output current of a SEPIC H-bridge inverter

Roy Fada Krisna Wisnu Mahendra[1,*], Leonardus Heru Pratomo[2]
[1,2]Department of Electrical Engineering, Soegijapranata Catholic University
[1]Pawiyatan Luhur Street, No. 1, Semarang 50234, Indonesia
[*]Corresponding email: krisnamahendra522@gmail.com

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Abstract — The rapid depletion of fossil fuels and humanity's increasing dependence on electricity drive us to adopt renewable energy-based power generation. However, using renewable energy requires a system to maximize the results of converting renewable energy into electrical energy. An inverter is a DC-to-AC power conversion device. Inverters have two types: buck and boost. In closed-loop control, it can be controlled using current or voltage control. Current-controlled inverters sent to the grid have constraints, such as the inverter input voltage value must exceed the voltage on the grid. This study suggests using an H-bridge inverter and an AC-AC SEPIC to generate a voltage value more significant than the input voltage value. The proposed converter uses a single DC source and bases grid current injection on the regulated output current approach. The proposed converter satisfies the IEEE Std 519-2014 requirement of less than 5 % and has a Total Harmonic Distortion (THD) of 4.6 %.

Keywords – buck-boost, current control, H-bridge Inverter, injecting current into the grid, SEPIC converter

I. Introduction

The depletion of fossil fuels is accelerating, and the growing reliance of human lifestyles on electricity is compelling us to transition towards electricity generation that relies on renewable energy sources, such as solar photovoltaic (PV) solar cells [1]. Solar photovoltaic (PV) cells integrated with grid-connected inverters offer a viable solution to the challenges posed by non-renewable energy sources, as they can help meet the growing global energy requirements [2], [3]. A grid-tied inverter is an inverter that has a current-controlled control system and can be used to transmit current to the grid. In a current-controlled inverter configuration, the current is typically connected in parallel with the output impedance, and it is also connected in parallel with the grid, which acts as a voltage source. The grid impedance is then connected in series with this arrangement. Controlled current can be obtained from a voltage source inverter with a current-controlled control system in its switching [4]. The current control strategy of the grid-tied inverter can reduce the harmonics of the current delivered to the grid [5]. Current-source inverters require a high-value input DC-link inductor, which restricts the current ripple in the DC source. Current-source inverters have short-circuited DC-link inductors to obtain enormous power [6]. In this operational mode, the current source inverter can be called a "boost inverter," as the output voltage consistently exceeds the input voltage. In contrast, the voltage source inverter can be characterized as a "buck inverter," as its output voltage is always lower than the input voltage [7]–[9]. However, current source inverters have some disadvantages in the number of semiconductor components that are more numerous and require a sizeable dc-link inductor size so that the dc- link current remains almost constant than voltage source inverters and lower efficiency values compared to voltage source inverters [10], [11]. With a current-controlled control system, the voltage source inverter can compensate for the grid's unbalanced current so that when a load disturbance occurs, the current on the grid can be stabilized [2], [12].

To enhance the low DC input voltage and construct buck-boost inverters for integrating renewable energy sources, conventional Voltage Source Inverters (VSI) frequently have DC-DC boost converters such as Fly-back, Cuk, and SEPIC converters added to them. This topology involves double power processing (a two-stage inverter) and utilizes an H-bridge switching pattern. The two-stage inverter is proposed by [13]. Using

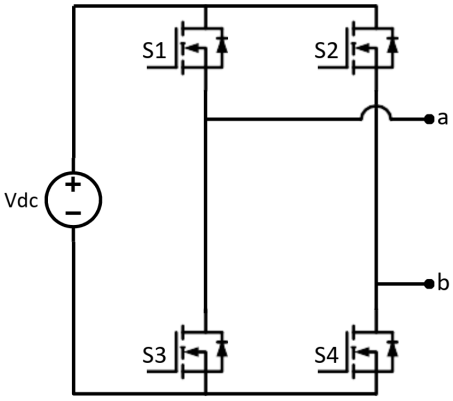

Fig. 1. Inverter H-bridge.

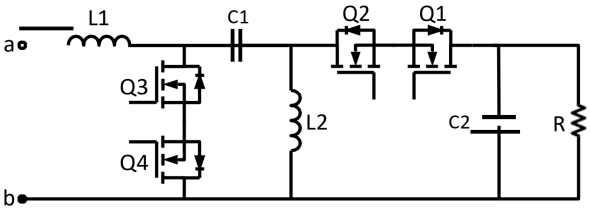

Fig. 2. AC-AC SEPIC.

five active switches has several disadvantages, such as an increased number of semiconductor components and requiring a high DC bus voltage at the input, causing control complexity [14], [15].

Several studies have introduced novel inverter topologies to streamline the control complexity and minimize the number of components in DC/AC converters. One notable approach is the development of closed-loop control circuits for single-stage active buck-boost inverters. These innovative designs incorporate fewer passive components [16]–[18]. Additionally, [19], [20] presents simulation results for a single-stage inverter employing only four active switches coupled with an AC-AC buck-boost inverter. These efforts aim to enhance the efficiency and simplicity of DC/AC conversion systems.

In this paper, a new topology is introduced, the use of current controlled voltage source inverter in the form of an H-bridge SEPIC inverter with four active switches with single stage buck-boost inverter topology through combining H-bridge inverter with AC-AC SEPIC active. The maximized benefit of the proposed topology is a better output waveform than the buck-boost inverter type. A single-stage H-bridge SEPIC inverter is more efficient than a two-stage inverter, which has many disadvantages and uses a controlled current control strategy.

II. Research Method

This section discusses the circuit schematic, operation mode, current control system, and the current control strategy of the proposed topology.

A. Circuit Schematic

Fig. 1 is the power circuit of an H-bridge inverter that uses four active switches (S1-S4). Fig. 2 is the power circuit of the AC-AC SEPIC, which includes four active switches (Q1-Q4). Fig. 3 is a schematic of the proposed circuit, namely Fig. 1 and Fig. 2, connected through points "a" and "b". The SEPIC H-bridge Inverter uses eight active switches (S1-Q4), two inductors (L1-L2), and two capacitors (C1-C2). The SEPIC H-bridge Inverter operates in buck mode and boost mode. The H-bridge inverter generates the buck mode with an output range of $V_{ab} < V_{dc}$. The AC-AC SEPIC generates the boost mode, which can expand the output voltage range to above V_{dc}.

B. Operation Mode

The proposed topology is shown in Fig. 3, with two parts: An H-bridge inverter and AC-AC SEPIC. This topology uses an H-bridge inverter with a single DC source, which will produce an output of $V_{ab} = V_{dc}$, 0, - V_{dc}. On the H-bridge inverter side, the pulse width modulation (PWM) method with unipolar switching triggers active switches S1 and S3, while S2 and S4 will work as zero-crossing detectors.

A carrier signal is required in the proposed H-bridge inverter topology. There are modulation signals that are sinusoidal, namely "PI" (blue color) and "-PI" (green color). Fig. 4 explains the modulation technique between the carrier and sinusoidal modulation signals (PI) and (-PI). When the proportional-integral (PI) control value is positive, it signifies the desire for switch S1 to be active. This action ensures that the output voltage is positive and helps drive the error value toward zero. When the proportional-integral (PI) control value is negative, it indicates the intention for switch S3 to be active. This arrangement is designed to result in a negative output voltage, and it helps drive the error value toward zero. So that switch S1 is active when the PI value is positive, the PI value is modulated to a positive carrier signal. So that switch S3 is active when the PI value is negative, the PI signal needs to be inverted by multiplying it by -1 and the resulting -PI signal so that if the PI value is negative, the -PI value is positive and vice versa with the same amplitude. If the -PI signal is modulated to the same carrier, an SPWM signal is generated whose phase is shifted 1800 with the SPWM signal used for switch S1, as shown in Fig. 4.

Fig. 5 shows the low-frequency switching process to control switches S2 and S4 in the inverter. Switch S2 is active only when the PI value is negative or -PI. This switch is active during the SPWM switching process of switch S3. When the two switches are active, a negative voltage will be generated at the load so that the load current drops and will increase the error value. Switch S4 is active only when the PI value is positive; this switch is active during the SPWM switching process of

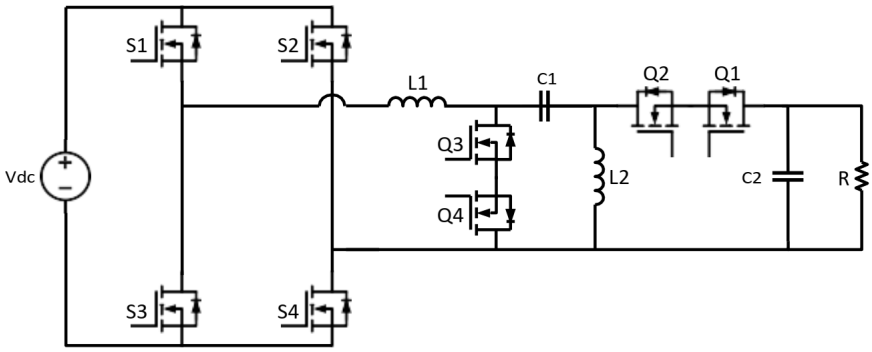

Fig. 3. SEPIC H-bridge inverter.

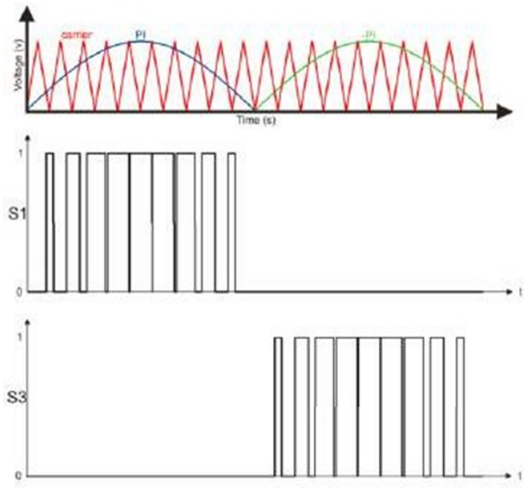

Fig. 4. Modulation of PI and -PI signals to the carrier.

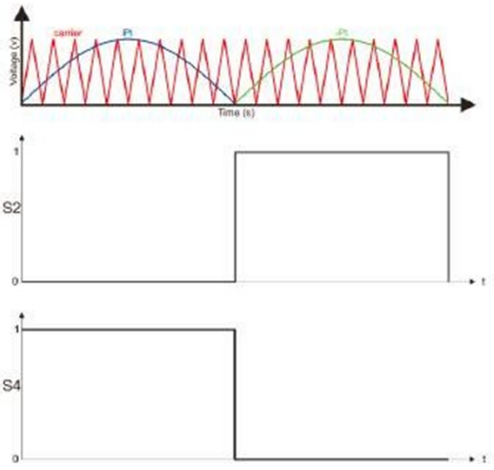

Fig. 5. Zero-crossing detection-based switching.

switch S1. When the two switches are active together, a positive voltage will be generated at the load so that the load current rises and will decrease the error value. Table 1 describes the switching operations of the H-bridge inverter.

Table 1. Switching in Buck Mode of Operation

S1	**S2**	**S3**	**S4**	V_{ab}
S1	S2	S3	S4	V_{ab}
1	0	0	1	V_{dc}
0	0	0	1	0
0	1	0	0	0
0	1	1	0	$-V_{dc}$

When $V_{ab} = V_{dc}$, the active switches on the working part of the H-bridge inverter are S1 and S4. Then, when $V_{ab} = -V_{dc}$, the active switches on the working H-bridge inverter section are S2 and S3.

Then, two bi-directional switches are in the AC-AC SEPIC section (Q1-Q2 and Q3-Q4). Fig. 6 presents the PWM method that triggers the active switch (Q1-Q4) on the AC-AC SEPIC. Two comparators are used, one to compare the value of V_d with the carrier value. The value of V_d regulates the duty cycle on "d," with the amount of duty cycle changing, it affects the range of the resulting voltage increase. One of the other comparators is used to generate zero-crossing, which helps determine the polarity of the voltage on the AC-AC SEPIC. AC-AC SEPIC works in two modes, namely buck mode and boost mode. In buck mode, the value of $V_d >$ peak carrier; this makes the "d" value have a duty cycle = 100 %. Then, in boost mode, the value of V_d is $0 < V_d <$ peak carrier.

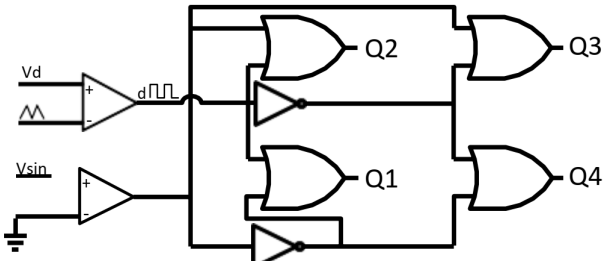

Fig. 6. AC-AC SEPIC modulation strategy.

Table 2. AC-AC SEPIC Switching

Mode	**Q1**	**Q2**	**Q3**	**Q4**	**Output**
Buck	$\bar{d}$	1	d	1	Half cycle (+)
	1	$\bar{d}$	1	d	Half cycle (-)
Boost	$\bar{d}$	1	d	1	Half cycle (+)
	1	$\bar{d}$	1	d	Half cycle (-)

The description of AC-AC SEPIC switching can be seen in Table 2, "1", representing the active switch's ON condition. At the same time, "d" and "$\bar{d}$" are the switching conditions obtained from modulating V_d with the carrier signal.

During positive half-cycle buck mode, Q2 and Q4 will always be ON, and Q1 will be opposite to Q3 with trigger "d". While during the negative half cycle,

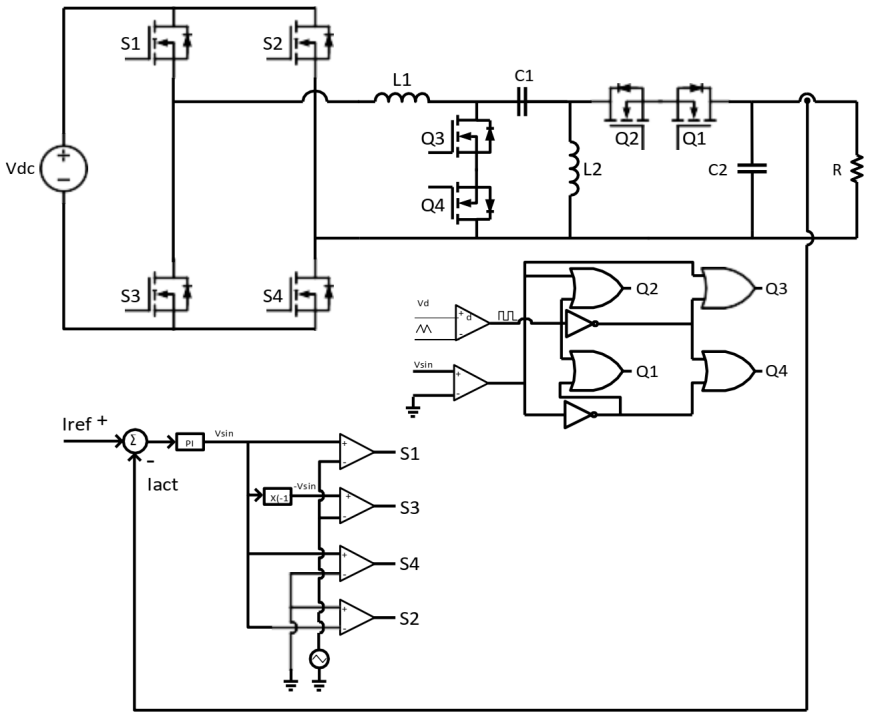

Fig. 7. The control scheme of the current-controlled SEPIC H-bridge inverter.

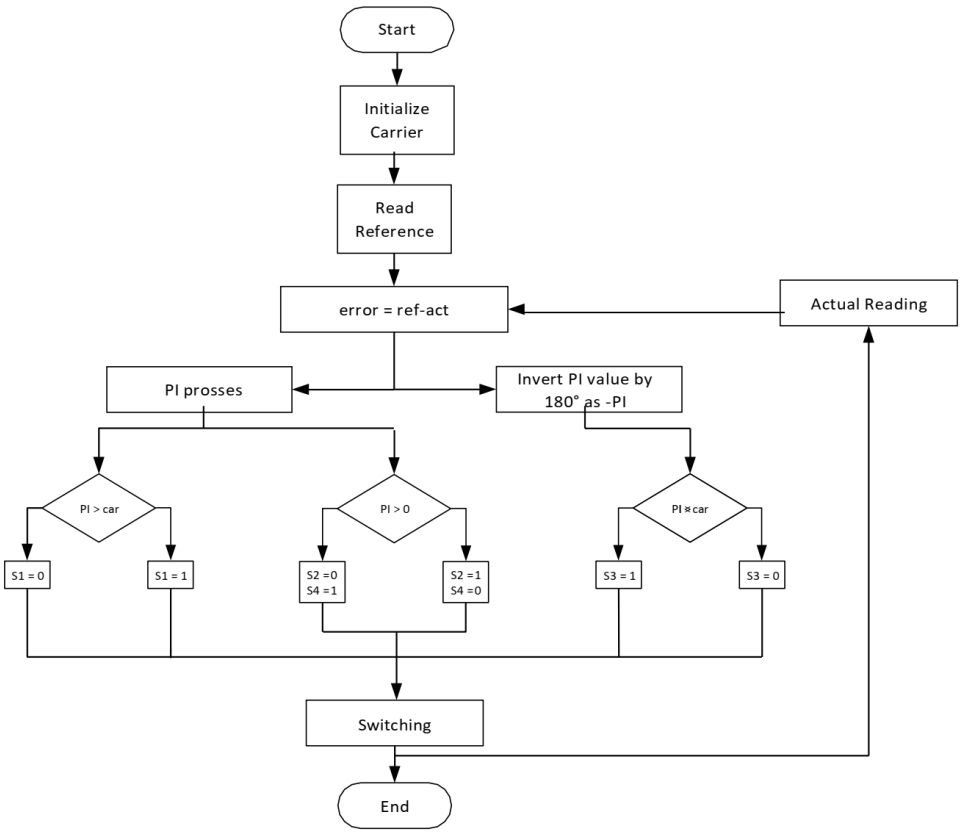

Fig. 8. Flowchart of current control on the proposed topology.

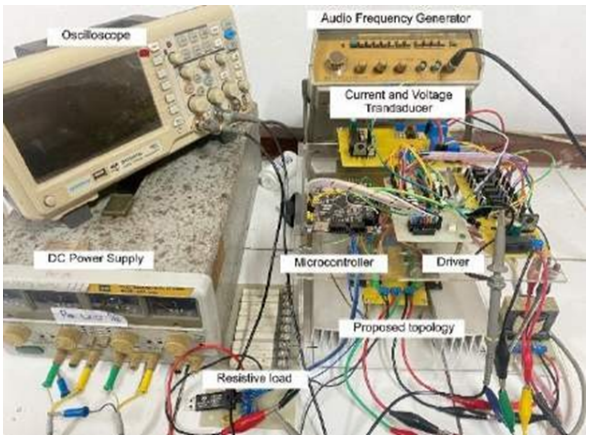

Fig. 9. Implementation of the proposed topology on hardware.

Q1 and Q3 will always be ON, Q2 will be opposite to Q4. Similar to the buck condition, in boost mode, during the positive half cycle, Q2 and Q4 switches are continuously turned ON, then Q1 will be opposite to Q3 with trigger "d." While the negative half cycle, Q1 and Q3 will always be ON, Q2 will be opposite to Q4.

C. Current Control System

In this study, the closed-loop system utilizes current control, and this control is achieved through the use of a proportional-integral (PI) controller. Implementing current control allows the injected current into the grid to be maintained constantly, even in load disturbances or changes. This ensures the stability and reliability of the system's current output.

Fig. 7 shows a current-controlled SEPIC H-bridge inverter control system with a zero-crossing detector. The reference current, which acts as the proportional-integral (PI) control input, starts the process. The error signal for this control mechanism is generated by subtracting the reference value and the actual value. The error signal for this control mechanism is generated by subtracting the reference value and the actual value. The error value is controlled by PI control for power switch control with a sine- shaped PI output value V_{sin}. Then, the PI controller output is modulated to a carrier signal to produce a PWM signal for controlling power switches S1 and S3, which operate at high frequency. As for the control of S2 and S4 power switches, V_{sin} is compared with a zero value to produce a zero-crossing output. V_{sin} is also used to control the AC-AC part of the SEPIC, where the V_{sin} value is compared with the zero value, with the comparison results entered into the logic gate circuit. To assess the effectiveness of this control scheme, testing is conducted by introducing load variations on the output side. This test aims to demonstrate that the output current of this topology remains stable even in the presence of load changes or disturbances. The algorithm detailing the current control strategy for this topology is presented in Fig. 8.

D. Current Control Strategy of the Proposed Topology

This section elaborates on the current control strategy of the proposed topology. The primary objective of this proposed topology is to introduce a device capable of injecting current into the grid while maintaining a low total harmonic distortion (THD) value and the capability to achieve an output voltage that surpasses the DC source voltage used as input. For the proposed topology to inject current into the grid, a control system is required to make the proposed topology current-controlled. Therefore, Fig. 7 shows the flowchart illustrating the current control method implemented in the proposed topology.

Fig. 8 represents a flowchart outlining the current control method employed in the proposed topology. The concept of current control in a converter is to obtain an error value $\approx$ of 0. The error value is obtained from the subtraction between the reference value and the actual value. A PI controller generates a modulation signal received from the PI calculation with the error value. The modulation signal will be compared with the control system of the converter and produce a PWM pulse as a trigger for the active switch of the proposed converter.

III. RESULT

Laboratory experiments were carried out to verify the analysis and simulations obtained from the study of the proposed topology. All simulations were implemented using Power Simulator Software. Table 3 presents the parameters used in the hardware implementation.

Table 3. Hardware Implementation Parameters

Input voltage	12 Volt DC
Non-polar capacitor	30 μF, 10 μF
Inductor	1 mH
Resistive load	100 Ω
Switching frequency	5 kHz

Table 3 shows the parameters of the components used in the hardware implementation. The value of each component is intended on a laboratory trial scale. In the software simulation, several experiments were conducted with different component parameters to recognize the characteristics of the converter. The Farad value of the non-polar capacitor, the Henry value of the inductor, and the switching frequency depend on the desired output power.

Fig. 9 shows the laboratory experiment level hardware implementation of the proposed converter along with supporting devices such as an oscilloscope measuring instrument, variable and regulated DC power supply, audio frequency generator as variable I_{ref}, voltage, and current transducers as feedback for STM32F407VET6 microcontroller, a driver for MOSFET, and resistive load.

Fig. 10 presents the output voltage waveform from the proposed converter after undergoing filtering, followed by the output current waveform. Additionally,

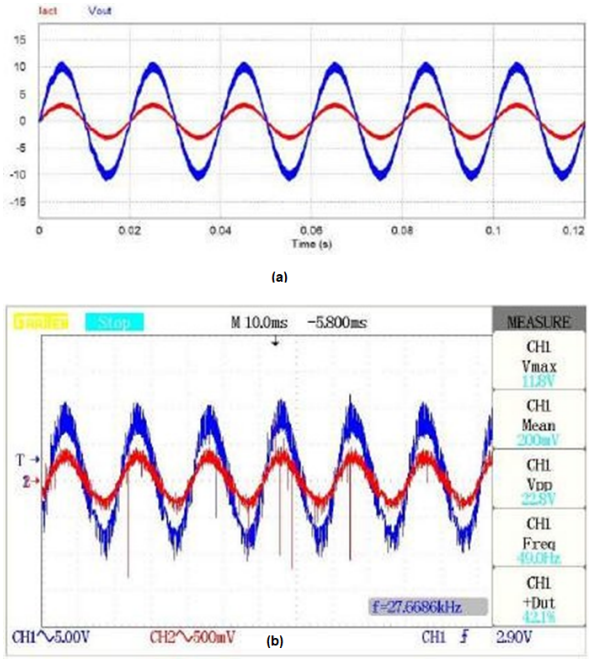

Fig. 10. Buck state output voltage and current (a) simulated waveform (b) implemented waveform.

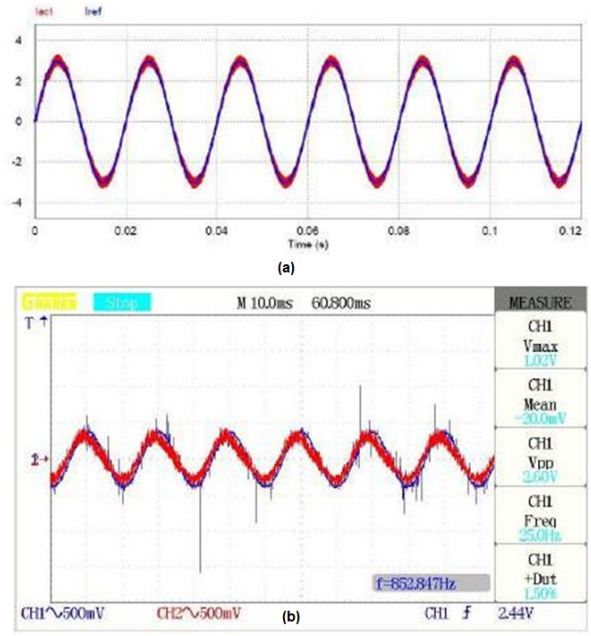

Fig. 11. Comparison between I_{act} and I_{ref} under buck condition (a) simulated waveform; (b) implemented waveform.

Fig. 10 (b) illustrates the waveforms obtained from the voltage and current transducers when operating under buck conditions.

Fig. 11 displays the implementation results of the current control strategy for the proposed converter. The current control has been simulated, and the findings indicate that the load current (I_{act}) can effectively track the reference value (I_{ref}). Fig. 11 (b) shows the waveforms obtained from the audio frequency generator as I_{ref} and the current transducer I_{act} under buck condition.

Fig. 12 presents that, in the buck state, the proposed

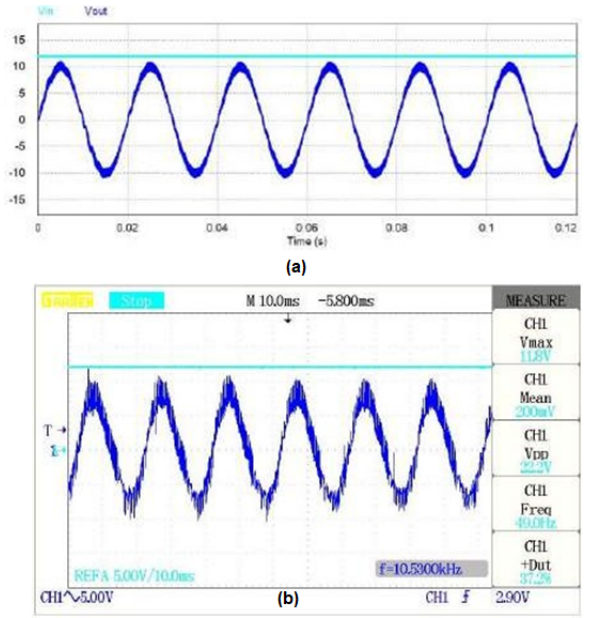

Fig. 12. Input and output voltage in buck state (a) simulated waveform (b) implemented waveform.

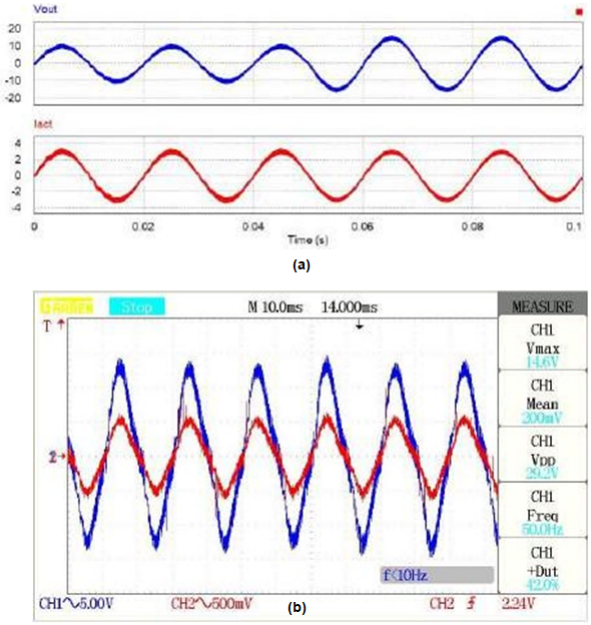

Fig. 13. Response of output voltage and current to load changes in buck condition (a) simulated waveform (b) implemented waveform.

converter can generate a waveform lower than the input voltage.

Laboratory experiments were conducted to evaluate how the proposed converter responds to a change in resistive load, where the resistive load was varied from 100 Ω to 50 Ω. Fig. 13 displays the proposed converter's current and voltage waveform responses during buck mode. In the presence of a load change, it is observed that the current waveform remains unchanged. In contrast, the output voltage waveform adjusts to align with I_{act} (actual current), which is required to track I_{ref} (reference current). This behavior indicates that the system effectively regulates the current to meet the desired reference value while adapting the output

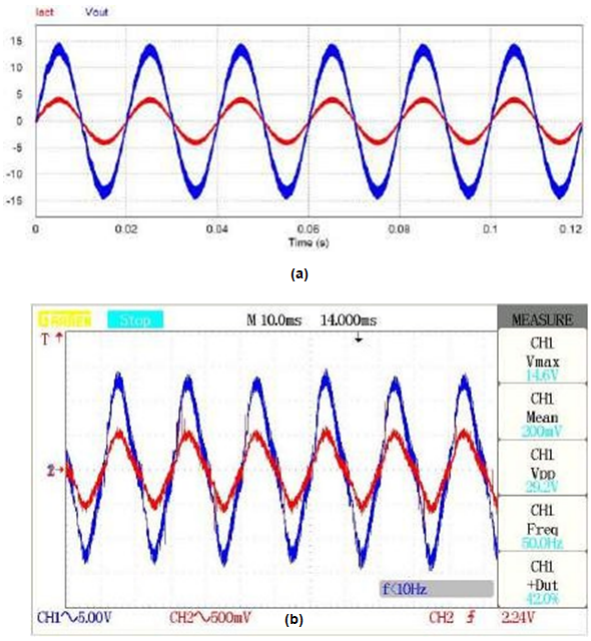

Fig. 14. Output voltage and current under boost condition (a) simulated waveform (b) implemented waveform.

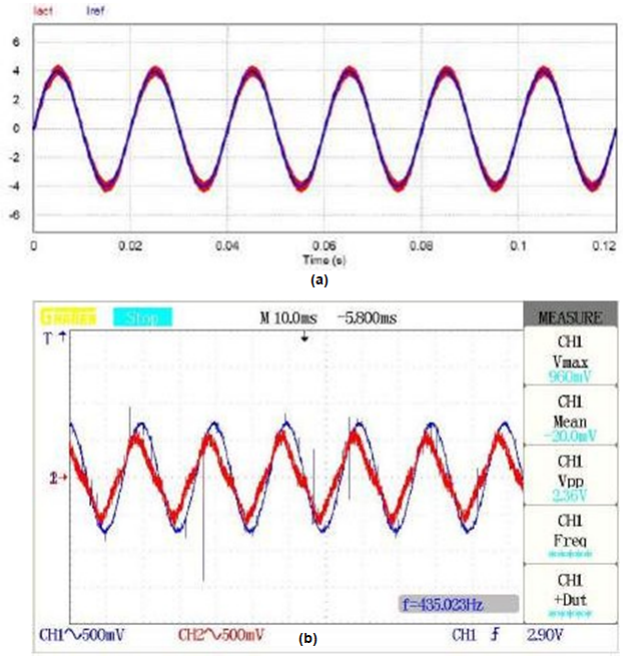

Fig. 15. Comparison between I_{act} and I_{ref} under boost condition (a) simulated waveform (b) implemented waveform.

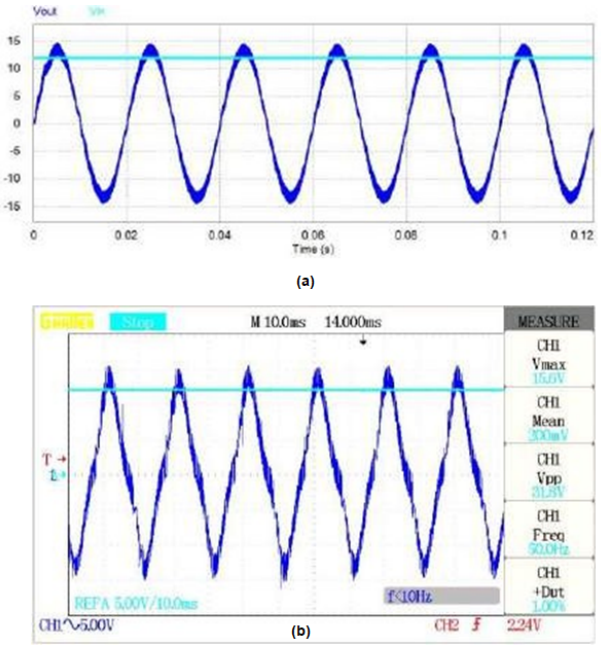

Fig. 16. Input and output voltage under buck condition (a) simulated waveform (b) implemented waveform.

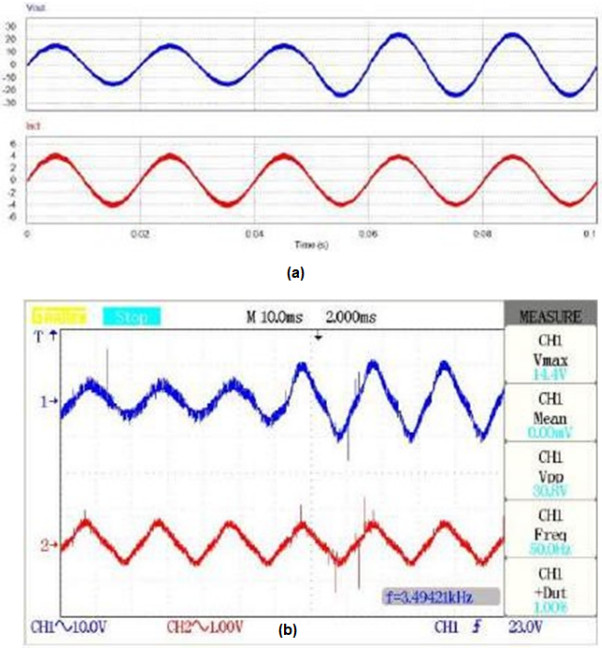

Fig. 17. Response of output voltage and current to changes in boost condition load (a) simulated waveform (b) implemented waveform.

voltage accordingly to maintain this current control. With the load current unchanged against the change in resistive load, the current in the proposed converter can also cope with external disturbances such as a changing V_{dc} value or I_{ref} value. The results of laboratory experiments to test the current controllability of the proposed buck state converter topology are shown in Fig. 13.

Fig. 14 displays the output voltage waveform from the proposed converter after undergoing filtering, followed by the output current waveform. Fig. 14 (b) presents the waveforms obtained from voltage and current transducers when the system operates in boost conditions.

Just like the buck condition, Fig. 15 shows that the current control in the simulation and implementation of the tool gets the result that the load current (I_{act}) can follow the reference value (I_{ref}).

Fig. 16 presents that the proposed converter can generate a waveform that exceeds the input voltage during the boost mode. This demonstrates that the proposed converter has an extended output voltage range when operating in boost mode. Selecting non-polar capacitor filter values (C1 and C2) is crucial in getting a good output shape. The smaller the farad

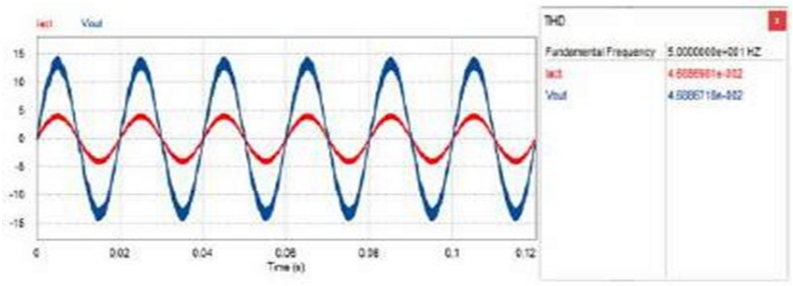

Fig. 18. THD values in output voltage and current.

value of the non-polar capacitor filter, the wider the ripple in the output voltage of the proposed converter.

The output voltage and current of the proposed converter topology produce a THD value of 4.6 %, as shown in Fig. 18. This value meets the IEEE Std 519- 2014 standard of less than 5 %. A low THD value is needed to inject current into the grid

IV. Discussion

Hardware implementation is carried out to prove that the H-bridge inverter combined with AC-AC SEPIC can work buck and boost following the simulation in PSIM. In research [13] using a two-stage inverter topology, this topology has the weakness of power processing twice. The topology can be overcome by applying a single-stage H-bridge inverter topology, using an H-bridge inverter combined with an AC-AC SEPIC, as shown in Fig. 3. The inverter only performs power processing once. The design of AC-AC SEPIC using the switching method is shown in Table 2. In the buck mode generated by the H-bridge inverter, as indicated in Fig. 12, the output voltage of the H-bridge inverter exhibits a reduction from an input voltage of 12 V to an output voltage of 11 V. Fig. 13 depicts a disturbance response test conducted on the H-bridge inverter load, where the resistive load varied from 100 Ω to 50 Ω. The objective of this test was to observe the changes in the output voltage waveform. The results show that the current waveform remains stable and unchanged throughout the load resistance variations. This happens because the proposed H-bridge inverter uses a current-controlled control system so that the current on the grid can be stabilized when there is a disturbance in the load. Then, the reference current and actual current in the buck condition can be tracked, as shown in Fig. 11.

Likewise, for the boost mode generated by AC-AC SEPIC with an input voltage of 12 V, the output voltage can be increased to 14 V, as shown in Fig. 16. Like the buck condition, when testing the response to the boost condition, the current wave is not affected when trying the load response from 100 Ω to 50 Ω, which changes the output voltage, as shown in Fig. 17. Then, the reference current and actual current can be tracked, as shown in Fig. 15. Then, the H-bridge topology with AC-AC SEPIC using a controlled current system can suppress harmonics at the output of 4.6 % so that it can be used for injecting current into the grid.

V. Conclusion

This paper introduces a new DC-AC topology combining an H-bridge inverter with a SEPIC AC-AC converter. According to the analysis and test results of the suggested converter, there are notable advantages, one of which is the expansion of the output voltage range achievable through the SEPIC AC-AC converter. The proposed converter has a control system on the output current. Therefore, the output current of the proposed converter will consistently track the reference current waveform. With controlled current, the proposed converter can overcome external disturbances such as changing V_{dc} or I_{ref} values. The benefits of a controlled output control current system and low THD value can be used in injecting current into the grid. The resulting THD value is 4.6 % and meets the IEEE Std 519-2014 standard of less than 5 %.

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