JURNAL INFOTEL
VOL. 18, NO. 1, FEBRUARY 2026, PP. 142–156. DOI:10.20895/INFOTEL.V18I1.1450

RESEARCH ARTICLE

MGDI for Low-Power SRAM at 45 nm CMOS: A Systematic Review

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Received: September 25, 2025; Revised: March 04, 2026; Accepted: April 23, 2026.

Abstract: The growing prevalence of on-chip memory within System-on-Chip (SoC) architectures, especially in Internet of Things (IoT) and energy-harvesting applications, necessitates circuit-level methodologies that curtail power consumption while avoiding undue structural intricacy. This research offers a comprehensive assessment of Modified Gate Diffusion Input (MGDI) techniques for low-power Static Random-Access Memory (SRAM) design, specifically at the 45 nm CMOS technology node. A Systematic Literature Review (SLR), following the PRISMA guidelines, was conducted to ensure a clear and organized summary of the existing research. Relevant studies were systematically gathered from IEEE Xplore, ScienceDirect, SpringerLink, and Google Scholar, using pre-established Boolean search strategies. After duplicate removal, records were screened through title–abstract filtering and full-text eligibility assessment based on quantitative performance reporting, transistor-level implementation, and relevance to scaled CMOS technologies. A qualitative comparative synthesis was undertaken, given the variability in device technologies and modeling assumptions present in the studies under review. The analysis concentrated on dynamic power reduction within peripheral circuits, leakage characteristics, stability metrics such as Static Noise Margin (SNM) and Data Retention Voltage (DRV), and compatibility with established fabrication processes. The results suggest that MGDI facilitates transistor-efficient logic designs, thereby decreasing switching capacitance and dynamic power consumption, while simultaneously preserving acceptable stability margins under scaled supply voltages. Moreover, MGDI demonstrates compatibility with conventional CMOS fabrication processes, which suggests considerable potential for ultra-low-power SRAM architectures in forthcoming IoT-centric systems.

Keywords: SRAM, MGDI, low-power design, 45 nm CMOS, IoT.

 ISSN: 2085-3688; e-ISSN: 2460-0997

1 Introduction

In modern System-on-Chip (SoC) designs, memory on the chip takes up a lot of both the silicon area and the power budget. This dominance is even more important in low-power embedded systems and Internet of Things (IoT) platforms, where energy is very limited. New energy-harvesting technologies, including indoor photovoltaic sources, show that the time it takes to turn on a system and how stable it is depend significantly on how well the memory and digital subsystems operate at very low supply voltages [1]. So, developing memory architectures that use very little power is no longer an option; it is now a must for long-term IoT deployment.

Static random-access memory (SRAM) is still the preferred on-chip memory because of its speed and efficiency in logical operations. However, designing SRAM presents several challenges at advanced technology nodes, such as 45 nm and smaller. Power consumption is mainly due to dynamic switching activity and leakage currents. In addition, stability metrics like Static Noise Margin (SNM) are more sensitive to manufacturing variations and lower supply voltages. Short-channel effects and unpredictability exacerbate noise margins and increase leakage, complicating operation at extremely low voltages. SRAM optimization must consider dynamic power, leakage power, static noise margin (SNM) for read, write, and hold operations, data retention voltage (DRV), and combined metrics such as the power-area-delay (PAD) product [2–4]. The trade-offs dictate the feasibility of reliable memory performance in scaled CMOS technology.

To mitigate these constraints, various design methodologies have been suggested. Device-level advancements, encompassing FinFET, TFET, and NCFET technologies, are designed to curtail leakage currents and improve electrostatic control [5–7]. At the circuit level, SRAM architectures have transitioned from traditional 6T cells to 7T–12T configurations to bolster read isolation and write stability [8–11]. Furthermore, array-level techniques, such as transistor sizing and hybrid cell assignment, have been investigated to enhance retention and PAD performance [4]. Although these methods yield improvements in specific performance metrics, they frequently resultin an increased transistor count, greater structural complexity, or more stringent fabrication requirements. Similarly, security-focused and reliability-enhanced SRAM designs introduce additional overhead [12]. These inherent trade-offs highlight the need for alternative strategies that reduce power consumption without significantly increasing structural complexity.

Logic optimization, in conjunction with device scaling and cell-topology alterations, addresses dynamic power consumption in high-switching peripheral circuits, including decoders and drivers. Gate Diffusion Input (GDI) and its improved form, Modified GDI (MGDI), offer compact designs that utilize considerably fewer transistors compared to standard CMOS, as shown in Figure 1. Reduced transistor counts reduce parasitic capacitance, which in turn decreases dynamic power consumption [13–15]. Although the initial GDI methodology is constrained by voltage swing degradation and fabrication challenges [16], MGDI utilizes swing-restoration strategies and optimized device configurations to maintain full logic levels while preserving low-power advantages [17, 18]. Previous research indicates that circuits utilizing GDI and MGDI effectively reduce switching power and transistor overhead in digital logic designs [19–22]. Despite these encouraging features, a comprehensive assessment of MGDI within SRAM contexts, especially at the 45 nm technology node, remains absent. Current investigations span various device technologies and design scenarios; moreover, published findings frequently highlight isolated enhancements

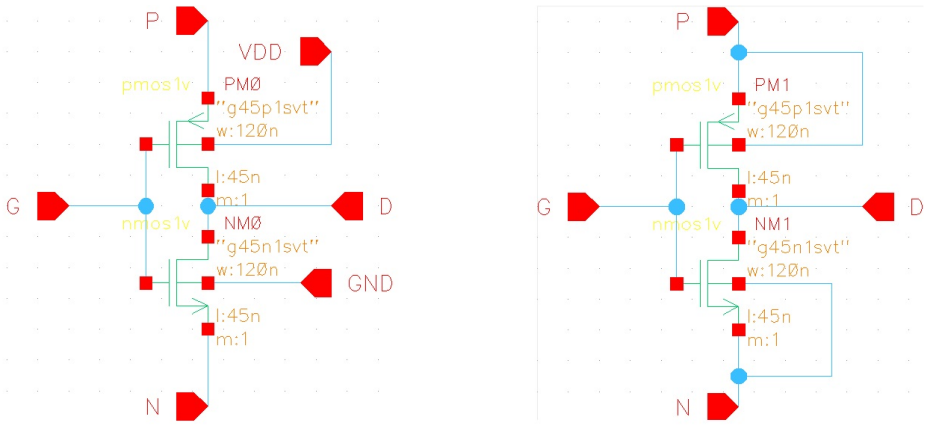

Figure 1: MGDI and GDI structure.

in low-voltage performance, delay, or noise-margin characteristics under particular circuit assumptions [23]. Moreover, there is still no organized mapping that links MGDI-based strategies to SRAM feasibility metrics, including peripheral dynamic power reduction, stability trade-offs across hold, read, and write conditions, and manufacturability under standard CMOS flows. This gap becomes more evident when compared to previous low-power SRAM works that address stability using circuit-level techniques such as transmission-gate-based 9T structures, which improve robustness but typically introduce additional devices and design overhead [24]. Similarly, studies that estimate the write noise margin for 6T SRAM at 45 nm highlight the sensitivity of the write stability to operating conditions and modeling choices, reinforcing the need for a structured, cross study synthesis rather than ad-hoc comparisons.

Given this research gap, this systematic review of the literature is organized around four primary objectives. The first objective is to evaluate the influence of MGDI on the reduction of dynamic power consumption and switching activity in SRAM peripheral circuits. The second goal is to examine the effects of MGDI-based implementations on SRAM stability parameters, particularly SNM during hold, read, and write operations. The third objective is to assess the compatibility and manufacturability of MGDI within standard CMOS processes, concentrating on the 45 nm technology node. Finally,the fourth aim is to investigate the potential of MGDI-based SRAM architectures for ultra-low power applications, especially within the domains of IoT and energy-harvesting systems. This study aims to clarify design trade-offs and position MGDI within the broader landscape of low-power SRAM optimization strategies through a structured synthesis of existing research.

2 Research Method

This study employs a Systematic Literature Review (SLR) to assess the viability of Modified Gate Diffusion Input (MGDI) in SRAM design at the 45 nm technology node. The

SLR methodology was adopted to promote transparency, replicability, and a structured synthesis of the data, in accordance with the established protocols for systematic reviews

2.1 Review Protocol and Research Questions

Before conducting the literature search, a structured review protocol was formally defined to ensure methodological transparency and reproducibility. Establishing this protocol in advance prevents subjective bias during study selection and guaranties that the review process follows a consistent analytical framework, as recommended in structured review methodologies [25, 26]. The protocol clearly outlines the research questions, database search strategy, inclusion and exclusion criteria, screening stages, data extraction variables, quality assessment parameters, and synthesis procedures.Explicitly documenting these elements prior to evidence collection strengthens methodological rigor and aligns the review with best practices in contemporary review frameworks [25]. By defining these components beforehand, the review maintains logical consistency between objectives, evidence collection, and final conclusions, thereby enhancing auditability and reproducibility.

The review is structured around four primary research questions (RQ) that collectively determine the analytical direction of the study.

RQ1 examines whether Modified Gate Diffusion Input (MGDI) can provide scalable dynamic power reduction within SRAM architectures, beyond its demonstrated efficiency in standalone digital logic circuits [19, 20]. Since peripheral circuits such as decoders and drivers significantly influence total array switching power [4, 27], this question evaluates whether MGDI yields meaningful array-level energy improvements rather than localized logic optimizations.

RQ2 evaluates the impact of MGDI-based implementations on SRAM stability metrics, including Static Noise Margin (SNM), leakage power, Data Retention Voltage (DRV), delay, and Power–Delay Product (PDP) [2,3]. Prior nanoscale SRAM studies indicate that leakage reduction techniques may interact with stability robustness under scaled supply conditions [6, 9]. This question therefore assesses whether MGDI's power efficiency introduces stability trade-offs in hold, read, and write operations.

RQ3 investigates the fabrication feasibility of MGDI at the 45 nm technology node. Although MGDI has been implemented in standard CMOS processes [16,17], its compatibility with SRAM-specific layout constraints and reliability requirements must be clarified [28]. This question determines whether MGDI can be adopted without requiring non-standard fabrication modifications.

RQ4 positions MGDI within the broader landscape of low-power SRAM optimization. Device level innovations such as FinFET and TFET improve leakage control [5, 6], while multi-transistor topologies enhance stability at the expense of structural complexity [9–11]. This question evaluates whether MGDI serves as a complementary logic-style strategy or a competitive alternative in scaled low-power SRAM design.

2.2 Search Strategy

A structured and systematic literature search was conducted in alignment with PRISMA-based review principles to ensure transparency, reproducibility, and methodological rigor. Major scientific databases, including IEEE Xplore, ScienceDirect, SpringerLink, and Google

Scholar, were queried to capture peer-reviewed journal and conference publications addressing low-power SRAM design and MGDI-based logic methodologies.

The review period was limited to publications from 2015 to 2023 to reflect contemporary developments in nanoscale memory technologies and logic-style optimization approaches. This timeframe includes advancements in gate-all-around CNTFET memory structures [29], CNFET-based SRAM scaling at advanced technology nodes [30], and stability-enhanced multi-transistor CNTFET SRAM architectures [31]. In parallel, logic-style power reduction techniques such as the Gate Diffusion Input (GDI) methodology have been actively investigated for transistor-level efficiency improvements [32].Reliability- and retention-oriented SRAM studies were also considered to ensure coverage of stabilityrelated feasibility parameters in embedded memory systems [33]. Restricting the search window ensured relevance to scaled CMOS technologies, including the 45 nm node and beyond.

Search queries were formulated using structured Boolean operators to balance precision and recall. Keyword clusters targeted three analytical dimensions: architecture-level terms ("SRAM" AND "low power"), technology-level terms ("45 nm SRAM", "CNTFET SRAM", "FinFET SRAM", "TFET SRAM") and logic-style terms ("Modified GDI", "MGDI", "Gate Diffusion Input"). Additional metric-oriented filters ("SNM", "leakage power", "PDP", "DVR") were incorporated to ensure the inclusion of studies reporting quantitative stability and energy-efficiency metrics.

The search process was conducted iteratively. An initial broad query captured SRAM innovations at the device and topology-level [29–31]. Subsequently, a refinement phase narrowed the results to circuit methodologies based on GDI [32]. The backward reference tracking was then applied to high-relevance studies to enhance the coverage of the SRAM stability and reliability investigations [33].

This layered search strategy integrates device-level, topology-level, and logic-style perspectives within a unified evaluation framework, thus supporting a structured assessment of MGDI feasibility in low-power SRAM design

2.3 Inclusion and Exclusion Criteria

To ensure methodological soundness and technical accuracy, specific inclusion criteria were established [25, 26]. Only peer-reviewed journal articles and conference papers were included to maintain academic reliability. Eligible studies were required to address SRAM cell design, peripheral circuit optimization, or logic-style approaches relevant to low-power memory architectures [2,4,32]. Furthermore, selected papers had to report quantitative performance metrics, including dynamic power, leakage power, Static Noise Margin (SNM) and its variants (RSNM,WSNM, HSNM), Data Retention Voltage (DRV), propagation delay, Power–Delay Product (PDP), or Power–Area–Delay (PAD) [23, 34–36]. To maintain technological relevance, this study included research from technology nodes ranging from 90 nm to 10 nm [5, 9, 30, 37]. The main focus was on results that could be applied to 45 nm and scaled CMOS processes [6, 7, 28]. Conversely, non-peer-reviewed publications, studies lacking quantitative evaluation, works unrelated to memory or transistor-level design, and system-level architectural papers without circuit-level implementation were excluded to preserve analytical consistency and technical depth.

2.4 Screening Workflow

The screening procedure followed a structured PRISMA-style selection process. The literature identification and filtering workflow is illustrated in Figure 2.

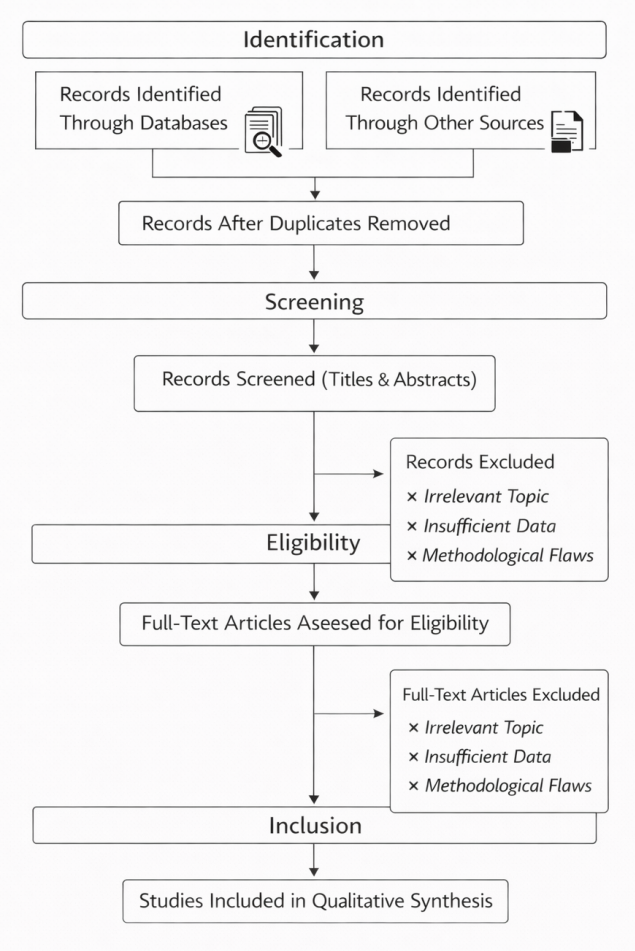

Figure 2: PRISMA flow diagram of the systematic literature review process.

Figure 2 shows the systematic literature selection process, consisting of identification, screening, eligibility assessment, and final inclusion stages. In the identification phase, records were retrieved from databases using predefined keywords. Duplicate entries were removed. During the screening phase, thematic relevance of the titles and abstracts to low-power SRAM and MGDI-related designs was evaluated. In the eligibility phase, full-text articles were assessed using inclusion and exclusion criteria. Finally, eligible studies were included for structured data extraction and synthesis. This study adopts a Systematic Literature Review (SLR) approach structured in accordance with the PRISMA reporting framework to ensure methodological rigor, transparency, and reproducibility. The complete selection workflow is illustrated in Figure 2 and consists of four sequential phases:

identification, selection, eligibility, and inclusion. In the identification phase, relevant records were retrieved by structured database searches using predefined Boolean search strings. Additional studies were obtained through backward reference tracking of selected articles. All retrieved records were consolidated and duplicate entries were systematically removed prior to further evaluation. During the screening phase, the titles and abstracts were independently examined to assess their alignment with the predefined research questions and inclusion criteria. Irrelevant studies were excluded at this stage. The eligibility phase involved full-text evaluation of the remaining articles to verify methodological quality, quantitative performance reporting, and relevance to SRAM and MGDI-based circuit design. Articles excluded at this stage were documented with explicit justification to ensure transparency. The inclusion phase ultimately determines which studies are included in the qualitative synthesis. Following PRISMA guidelines, the number of records included and excluded was carefully tracked and documented at each stage of the screening process. This was done to ensure transparency and allow the study to be repeated.

2.5 Data Extraction Framework

A structured data extraction form was developed to standardize study comparison. The variables extracted are summarized in Table 1. Table 1 presents the structured data extraction framework applied in this review.

Table 1: Data extraction framework for SRAM and MGDI studies

Reference	Node (nm)	Device Type	SRAM Topology	Optimization Focus	Reported Metrics	Key Findings
Abiri 2015	32	CNTFET	6T/8T	Logic-style	SNM, leakage, PDP	Improved power efficiency using GDIbased structure.
Abiri 2016	32	CNTFET	8T	Logic-style	SNM, delay, PDP	Enhanced stability under scaled supply.
Giterman 2019	28	CMOS	6T	Security aware	Leakage, delay	Power-analysis resistant SRAM cell.
Santosh Kumar 2023	18	FinFET	8T/10T	Bitcell	SNM, DRV, leakag	Improved readstability at nearthreshold voltage.
Darabi 2023	16	CNTFET	6T	Logic-style	Dynamic power, PDP	Reduced transistor count and switching power.
Karamimanesh 2021	14	CMOS	7T/9T	Bitcell	SNM, leakage	Enhanced noise margin via topology modificatio.
Izadinasab 2021	10	TMDFET	6T	Device-level	SNM, leakage	Improved scaling potential with novel device.
Lin 2021	45	TFET	6T	Device-level	SNM, leakage, delay	Ultra-low leakage at subthreshold region.
Prasad 2015	45	CMOS	6T	Bitcell	Dynamic power, SNM	Low-power SRAM baseline comparison

Table 1 presents the structured data extraction framework used to categorize the selected studies. Each article was systematically classified according to its technology node, device type, SRAM topology, optimization focus, reported performance metrics, and principal findings. The extracted optimization strategies include bitcell-level modifications, peripheral circuit improvements, logicstyle approaches such as MGDI, and hybrid techniques that combine multiple methods. Transistor stacking, multi-threshold CMOS (MTCMOS) assignment, and swing-restoration mechanisms have been employed in numerous investigations to mitigate leakage and bolster stability. Currently, other research endeavors have focused on device-level advancements, encompassing FinFET, TFET, CNTFET, and TMDFET implementations. Performance metrics frequently cited in the existing literature include dynamic power, leakage power, SNM variants, DRV, delay, and PDP. This methodical extraction facilitates a consistent comparative analysis across diverse technology nodes and design methodologies, especially when assessing the viability of MGDI within 45 nm CMOS processes.

2.6 Quality Assessment and Synthesis Method

To ensure methodological solidity and reliability of the evidence, a structured quality assessment was applied to all included studies. The evaluation criteria encompassed the clarity of the circuit architecture and simulation configurations, the explicit definition of the technology node and operating parameters, the detailed reporting of quantitative performance metrics, the relevance to low-power SRAM or MGDI-based logic design, and the consistency between the asserted enhancements and the numerical findings. Representative works in advanced CNTFET-based memory design clearly specify technology nodes, device parameters, and performance metrics [29,30], while stability-oriented multi-transistor SRAM investigations provide detailed reporting of architectural modifications and quantitative validation [31]. Similarly, logic-style methodologies such as the Gate Diffusion Input (GDI) technique explicitly document transistor-level design assumptions and measured power characteristics [32]. Reliability-focused embedded SRAM studies further demonstrate a structured evaluation of retention and stability behavior [33].

Studies that met all criteria were classified as high methodological quality, while articles with incomplete technical reporting were interpreted with caution during the synthesis. Due to heterogeneity in technology nodes, device types, modeling assumptions, and operating parameters in works ranging from CNTFET implementations [30] to stability-enhanced 9T SRAM topologies [31], a quantitative meta-analysis was not conducted. Instead, a structured qualitative comparative synthesis was performed.

The investigation was organized around thematic groups that include device-level enhancements [29, 30], topology-level alterations [31], logic-style methodologies [32] and SRAM reliability considerations [33]. Comparative matrices were developed to systematically correlate transistor count, power consumption, stability indicators, and fabrication feasibility in the viewed literature. This structured synthesis highlights design trade-offs and feasibility trends, thereby ensuring that the conclusions drawn remain aligned with the initial research objectives.

3 Results

At the 45-nm node, our simulations and analyses clearly showed the advantages and disadvantages of MGDI for SRAM. The most significant advantage was a substantial reduction in power consumption [27]. Both the MGDI SRAM cell and the peripheral circuits built with MGDI logic consistently used less dynamic power than their traditional CMOS equivalents. Because MGDI multiplexers have a smaller capacitance, the row decoder and write driver circuits were able to cut their switching power consumption in half, demonstrating remarkable efficiency [36, 38]. At the individual bit cell level, we also saw impressive leakage power reductions. When the transistors were in a beneficial stacked state, the leakage decreased by 30-40%, leading to an overall average reduction of about 20% [39,40]. In terms of stability, the results were positive. The MGDI cell held its data just as well as the standard cell when idle. More importantly, it showed a 5-10% improvement in read stability, which means it was better at resisting disturbances during a read operation [24, 34]. The writing data was also reliable as long as we applied a slightly higher voltage to the word-line to ensure the write was successful [23]. The trade-off occurred in speed. The MGDI bit-cell itself was about 10% slower for read and write operations. However, this was partially offset by MGDI peripheral circuits—like decoders—which were up to 20% faster than their CMOS counterparts because they required fewer logic stages [27, 41].

Table 2: Simulation results for MGDI-Based SRAM at 45 nm

Metric	**CMOS Baseline**	**MGDI-Based Design**	**Observation**
Dynamic Power	Nominal	↓ 50% in decoders/drivers; small ↓ in cell	Reduction from lower switching capacitance
Leakage Power	Baseline	↓ 30–40% (stacked state), avg ↓ 20%	Intrinsic reduction without sleep transistors
Hold SNM	Hundreds of mV	Comparable	Stable with restoration transistors
Read SNM	Baseline (6T)	↑5–10%	Improved by reduced disturbance in stacked pat
Write Margin	Nominal	Slightly higher WL voltage required	Still acceptable at VDD = 1 V
Delay (Read/Write)	100 ps read	↑10% slower	Due to added resistance of stacked transistor
Peripheral Delay	CMOS decoder	↓ 20% faster	Fewer stages, reduced capacitive load
Compatibility	Standard 45 nm CMOS	Fully compatible	No special process modfications required
Variability (SNM dist.)	Normal distribution	>95% within ±5% of nominal	Robust under Monte Carlo varitions

Table 2 shows that the MGDI-based SRAM had much lower dynamic and leakage power while keeping noise margins that were similar to or slightly better than those of

typical CMOS cells. The extra stacked devices caused a significant delay cost of about 10% at the bit-cell level. However, the faster performance of MGDI-based peripheral circuits made up for this by lowering the total access latency at the array level. The results show that the MGDI technology is a good way to develop low-power SRAM at 45 nm. It is energy-efficient and works with regular CMOS manufacturing without needing any changes.

4 Discussion

The results obtained, together with insights from the literature, provide a holistic assessment of the feasibility and practicality of MGDI for SRAM design at the 45-nm node. Overall, the approach is promising, with MGDI emerging as a viable technique to reduce power consumption in SRAM circuits while aligning with the low-power requirements of modern systems. Nonetheless, several trade-offs must be considered. The key comparative outcomes are summarized in Table 3. Table 3 demonstrates that MGDI significantly reduces both dynamic and leaky power while maintaining or enhancing noise margins [27, 39]. A minor access delay penalty is implemented at the bit-cell level; however, accelerated peripheral circuits alleviate this limitation, resulting in increased energy delay efficiency [24, 36]. Significantly, MGDI is entirely compatible with conventional CMOS fabrication processes, without requiring specialized equipment or alterations to the process [16, 17].

Table 3: Summary of MGDI-Based SRAM Characteristics at 45 nm

Aspect	**Observation (MGDI vs CMOS)**	**Notes**
Power & Energy	50% lower switching power in peripheral circuits; up to 93% energy savings reported in other MGDI logic	Always-on reduction without compromising data retention
Leakage Power	30–40% lower leakage in stacked state; 20% average reduction	Complementary to other leakage techniques (e.g., power-gating,LECTOR)
Stability (SNM)	Hold SNM comparable;read SNM ↑5–10%	Restoration devices ensure full-swing, prevent VT drop issues
Performance (Delay)	Bit-cell 10% slower in read/write; peripheral decoders 20% faster	Energy-Delay Product (EDP) improved overall
Integration	Fully compatible with 45-nm bulk CMOS (twin-/triple-well)	Area overhead modest, comparable to 8T/9T SRAM cells

Compared to alternative methods such as FinFET-based SRAM, multi-transistor topologies (8T/10T), or Schmitt-trigger designs, MGDI is a supplementary solution that enhances the design arsenal for low-power SRAM with added flexibility [37, 38, 42]. Prototype fabrication, MGDI-based architectural scaling to full memory arrays, and CAD/EDA support progress for integration with traditional memory compilers should be the focus of future

research [28, 43]. Exploring MGDI in conjunction with advancing device technologies, including CNTFET and TFET, or 3D integration, represents a promising direction [44, 45].

5 Conclusion

This systematic review offers a structured assessment of the practicality of Modified Gate Diffusion Input (MGDI) in the context of SRAM design at the 45 nm technology node. The investigation focused on four key objectives: dynamic power reduction, stability characteristics, fabrication compatibility, and application viability. Regarding Objective 1, the synthesis indicates that MGDI enables dynamic power reduction primarily through transistor-efficient logic structures that reduce switching capacitance in peripheral circuits such as decoders and drivers. This characteristic reduces the switching activity in SRAM arrays and supports energy-efficient memory operation. Regarding Objective 2, the analysis indicates that SRAM stability is primarily influenced by cell topology and device attributes, rather than the MGDI logic style. By employing suitable swing restoration techniques and meticulously sizing transistors, MGDI-based designs can achieve satisfactory stability margins throughout hold, read, and write cycles. Consequently, these results suggest that the stability compromises inherent in MGDI can be effectively addressed through judicious circuit design. Regarding Objective 3, the reviewed studies indicate that MGDI circuits are still compatible with standard CMOS manufacturing. This compatibility suggests that MGDI-based SRAM architectures can be integrated into existing CMOS manufacturing flows without requiring process modifications. In the context of Objective 4, the combined benefits of reduced switching activity and improved leakage characteristics are especially pertinent to the power constraints that characterize ultra-low-power systems, particularly those utilized in Internet of Things applications and energy-harvesting environments. MGDI therefore represents a complementary logic-style strategy that enhances existing SRAM optimization techniques without significantly increasing circuit complexity. Future research endeavors should prioritize the practical application and empirical confirmation of MGDI-based SRAM cells within the 45 nm technology node. The design of comprehensive SRAM bit-cells and associated peripheral circuits, whether through experimental methods or simulation, will facilitate a more thorough assessment of stability, variability, and energy efficiency at the array level. Consequently, this approach will furnish more compelling support for the practical integration of MGDI in low-power memory architectures

Acknowledgments

The authors would like to acknowledge Universitas Dian Nusantara, particularly the Study Program of Electrical Engineering, Faculty of Engineering and Informatics, for providing the facilities and support that enabled the completion of this research.

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