JURNAL INFOTEL
Informatics - Telecommunication - Electronics
Website: http://ejournal.st3telkom.ac.id/index.php/infotel
ISSN: 2085-3688; e-ISSN: 2460-0997

Analysis and small-signal modeling of simplified cascade multiphase DC-DC buck converter

Nungky Prameswari
Department of Electrical Engineering, University of Surabaya
Jl. Raya Kalirungkut, Surabaya 60293, Indonesia
*Corresponding email: nungkyprameswari24@gmail.com

Received 30 July 2022, Revised 21 September 2022, Accepted 23 September 2022

Abstract — Renewable energy plays an important role in recent life due to the limited supply of fossil energy as an energy source to generate electricity. However, in its utilization, the energy gained from these renewable sources has not been able to be utilized directly as a source of electricity since the electrical power produced needs to be transformed from one form to another first. One approach to the use of renewable energy is power electronics, which convert electrical energy effectively using semiconductor technology. A DC-DC power converter is one of the power converters that is frequently used in renewable energy applications. A step-down converter or buck converter whose output voltage is lower than its input is one of these converters. In its application, specifications of the buck converter are typically required in its use. But a thing that more crucial than the specs is the dynamic modeling of the power converter by small-signal analysis using state space averaging. This research presents the open-loop analysis and small-signal modeling of a modified DC-DC buck converter for low-output voltage and high-output current applications. The voltage ratio of the proposed topology is greater than the conventional buck converter and this converter's output also has less ripple. So, the proposed topology is suitable for applications involving renewable energy. The small-signal model analysis and operation theory are covered in great detail. Finally, PSIM conducts a simulation study to evaluate the performance of the suggested topology.

Keywords – buck converter, cascade, multiphase, small-signal

I. Introduction

In the last few years, renewable energy plays an important role in recent life due to the limited supply of fossil energy as an energy source to generate electricity. However, in its application, the energy obtained from these renewable sources has not been able to be used directly as a source of electricity because the electrical power produced needs to be converted from one form to another first. Besides that, much electrical equipment cannot work efficiently if it is directly supplied with available sources.

The problem of using renewable energy has been overcome by power electronics technology, namely by providing equipment that is capable to produce efficient electrical energy conversion, distribution, and transmission [1]. This can also be found in Distributed Generator (DG) system which is connected to a DC Microgrid, where the role of the power converter is needed to connect AC and DC power sources from Distributed Generators (PV, Wind, and fuel cells) to the DC bus and it is also necessary for interconnecting with the utility grid. So, it can be described the important role of power electronics technology in the use of renewable energy, which is as a tool to convert energy.

One of the power converters that are often implemented in renewable energy applications is a DC-DC power converter [2]–[5], one such converter is a step-down converter or buck converter. Certain specifications that are usually necessary for buck converters are the ability to step down the voltage with a large drop rate and the ability to produce large output currents with very low ripples. Various converter developments have been carried out in [6]–[16]. In 2021, the newest version of them has been proposed in [17] which is also research before this paper, to which the author of this paper also contributed to the research. In that study, the authors found a new simplified cascade multiphase DC-DC buck power converter as a modified buck converter for large current low voltage

applications.

Several multiphase DC-DC buck power converters are connected in cascade to achieve a very low voltage ratio and very small ripple. And to reduce the required number of components, the resulting cascade multiphase DC-DC buck power converter is then simplified. And through the optimization carried out, namely based on conduction losses, it is found that the simplified two-cascade four-phase buck converter is the topology that produces the lowest conduction losses. And the other version of the converter for the Boost power converter type has also been proposed [18]. Another thing that needs to be known about power converters is how to dynamically model the system [19]. A dynamic model to approximate the behavior of buck converter has been proposed by using many different modeling techniques, one of which is small-signal modeling by state space averaging [20]–[25].

This paper proposes simplified multiphase DC-DC buck converter analysis and small-signal modeling. Additionally, simulation outcomes are provided to support the proposed converter.

The format of this paper is as follows. The proposed topology will be discussed in section II. Sections III and IV provide the small-signal analysis and simulation findings for the proposed converter, respectively. Finally, section V offers a conclusion.

II. Research Method

A. Conventional Buck Converter

A Buck converter is a specific kind of chopper circuit that is made to have a lower output voltage than its input value. This converter primarily consists of energy storage components like a capacitor, an inductor, or both, as well as switching components like a transistor and a diode. There are two conditions that determine how this circuit functions. A fluctuating voltage will be produced by the inductor across its terminals in response to the changing current since the circuit's current is zero when the switch is in the off-state and will start to climb when it is in the on-state. The voltage over the inductor rises as the current flow slows down over time, raising the voltage across the load. During this time, the inductor stores energy in the form of a magnetic field.

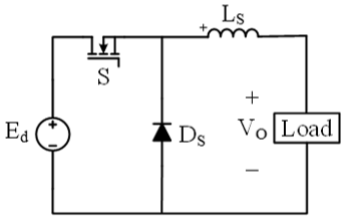

Fig. 1. Conventional step-down converter.

The conventional buck converter is seen in Fig. 1, and the voltage ratio is illustrated in (1), where the output voltage of the converter is denoted by V_o, the input voltage by E_d, and the fraction of one period in which semiconductor switches are active, namely duty cycle is denoted by α, which the letter T_S denotes the transistor's switching period and the ON-period denoted by T_{ON}. Although the duty cycle can be adjusted from zero to unity, it cannot be made too low in practice due to the switching device's minimum turn-off time.

$$\frac{V_o}{E_d} = \alpha \tag{1}$$

with,

$$\alpha = \frac{T_{ON}}{T_S} \tag{2}$$

B. Proposed Converter

Fig. 2 shows the optimal topology of the modified buck converter according to the optimization that has been done in the previous research [17]. The proposed converter consists of a DC source (E_d), two primary diodes (D_{1OFF}, D_{1ON}), four secondary diodes (D_1, D_2, D_3, D_4), four power switches (S_1, S_2, S_3, S_4), one capacitor (C), one primary inductor (L_p), and four secondary inductors (L_1, L_2, L_3, L_4). Since the output side of the topology is a four-phase buck converter, the suggested converter may provide huge output currents with extremely little ripple content. In (3), the average output voltage ratio is displayed, with the input voltage, output voltage, and duty cycle respectively denoted by the symbols V_o, E_d, and α.

$$\frac{V_o}{E_d} = 4\alpha^2 \tag{3}$$

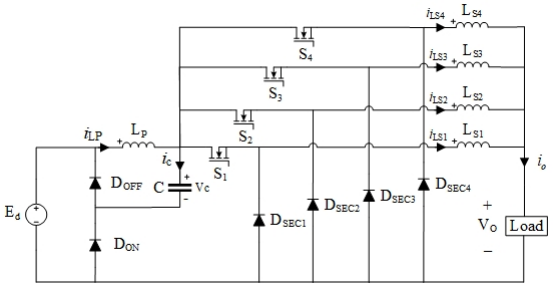

Fig. 2. Proposed converter.

Because the switch works alternately, assuming one conduction switch at time interval $0 \leq \alpha \leq 1/4$, there will be five operating modes, as indicated in Fig. 3 through Fig. 7, and the suggested converter's operating principle will be described as follows, where the description of the variables used in (1) to (16) is shown in Table 1.

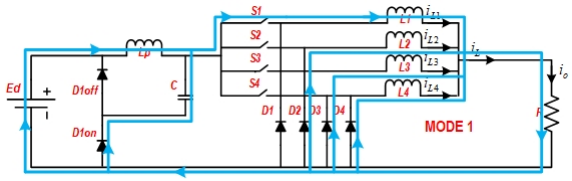

Fig. 3. Mode 1 (S1 is ON).

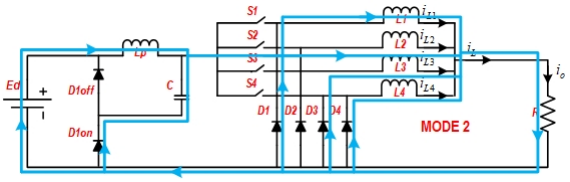

Fig. 4. Mode 2 (S2 is ON).

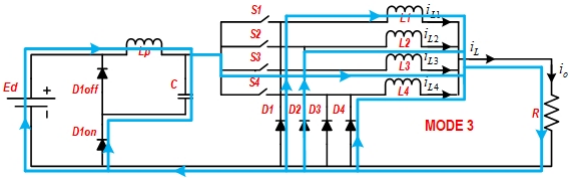

Fig. 5. Mode 3 (S3 is ON).

1) Mode 1, 2, 3, 4 (when one of the switch is ON)

During this procedure, one of the switches is ON. For example, the power switch S_1 is shown in Fig. 3. The other switches are off when S_1 is turned on. The primary diodes (D_{1ON} and D_{1OFF}) and every secondary diode besides D_1 will be forward biased in this situation, and current will flow from the DC source to primary inductor (L_p) and from primary diode D_{1ON} to capacitor C then the sum of the two currents will charge L_1. The other secondary inductors will let the current discharge before it reaches the load. The other switch conducts, as shown in Fig. 4 to Fig. 6, and the same thing occurs.

In mode 1 (when S_1 is ON) as an example, the voltage across the inductors L_p, L_1, L_2, L_3, L_4, and the capacitor C current can be expressed respectively as in (4) to (9). So that the state space mode 1 will be obtained as in (10).

$$\frac{di_{LP}}{dt} = \frac{E_d}{L_p} - \frac{V_C}{L_p} - \frac{R_{i_{LP}}}{L_p} \tag{4}$$

$$\frac{d_{i_{L1}}}{dt} = -\frac{i_{L1}R}{L_1} - \frac{i_{L2}R}{L_1} - \frac{i_{L3}R}{L_1} - \frac{i_{L4}R}{L_1} + \frac{V_C}{L_1} \tag{5}$$

$$\frac{d_{i_{L2}}}{dt} = -\frac{i_{L1}R}{L_2} - \frac{i_{L2}R}{L_2} - \frac{i_{L3}R}{L_2} - \frac{i_{L4}R}{L_2} \tag{6}$$

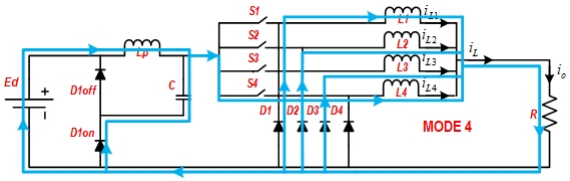

Fig. 6. Mode 4 (S4 is ON).

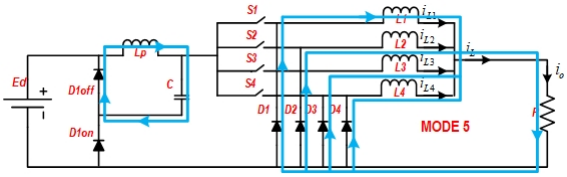

Fig. 7. Mode 5 (All switches are OFF).

$$\frac{d_{i_{L3}}}{dt} = -\frac{i_{L1}R}{L_3} - \frac{i_{L2}R}{L_3} - \frac{i_{L3}R}{L_3} - \frac{i_{L4}R}{L_3} \tag{7}$$

$$\frac{d_{i_{L4}}}{dt} = -\frac{i_{L1}R}{L_4} - \frac{i_{L2}R}{L_4} - \frac{i_{L3}R}{L_4} - \frac{i_{L4}R}{L_4} \tag{8}$$

$$i_C = i_{LP} - i_{L1} \tag{9}$$

$$\frac{d}{dt}\begin{bmatrix} i_{LP} \\ i_{L1} \\ i_{L2} \\ i_{L3} \\ i_{L4} \\ V_C \end{bmatrix} = \begin{bmatrix} -\frac{R}{L_p} & 0 & 0 & 0 & 0 & -\frac{1}{L_p} \\ 0 & -\frac{R}{L_1} & -\frac{R}{L_1} & -\frac{R}{L_1} & -\frac{R}{L_1} & 0 \\ 0 & -\frac{R}{L_2} & -\frac{R}{L_2} & -\frac{R}{L_2} & -\frac{R}{L_2} & 0 \\ 0 & -\frac{R}{L_3} & -\frac{R}{L_3} & -\frac{R}{L_3} & -\frac{R}{L_3} & 0 \\ 0 & -\frac{R}{L_4} & -\frac{R}{L_4} & -\frac{R}{L_4} & -\frac{R}{L_4} & 0 \\ \frac{1}{C} & -\frac{1}{0} & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{LP} \\ i_{L1} \\ i_{L2} \\ i_{L3} \\ i_{L4} \\ V_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L_p} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} E_d \tag{10}$$

Table 1. List of Variables

Variable	Description
E_d	Input voltage
α	Duty cycle
i_{LP}	Primary inductor (L_p) current
V_C	Capacitor (C) voltage
R	Load resistance
i_{L1}	Secondary inductor (L_1) current
i_{L2}	Secondary inductor (L_2) current
i_{L3}	Secondary inductor (L_3) current
i_{L4}	Secondary inductor (L_4) current
i_o	Output current

$$\frac{di_{LP}}{dt} = -\frac{V_C}{L_p} - \frac{Ri_{LP}}{L_p} \tag{11}$$

$$\frac{d_{i_{L1}}}{dt} = -\frac{i_{L1}R}{L_1} - \frac{i_{L2}R}{L_1} - \frac{i_{L3}R}{L_1} - \frac{i_{L4}R}{L_1} \tag{12}$$

$$\frac{d_{i_{L2}}}{dt} = -\frac{i_{L1}R}{L_2} - \frac{i_{L2}R}{L_2} - \frac{i_{L3}R}{L_2} - \frac{i_{L4}R}{L_2} \tag{13}$$

$$\frac{d_{i_{L3}}}{dt} = -\frac{i_{L1}R}{L_3} - \frac{i_{L2}R}{L_3} - \frac{i_{L3}R}{L_3} - \frac{i_{L4}R}{L_3} \tag{14}$$

$$\frac{d_{i_{L4}}}{dt} = -\frac{i_{L1}R}{L_4} - \frac{i_{L2}R}{L_4} - \frac{i_{L3}R}{L_4} - \frac{i_{L4}R}{L_4} \tag{15}$$

$$i_C = i_{LP} \tag{16}$$

2) Mode 5 (when all of the switches are OFF)

The other scenario is illustrated in Fig. 7, where all switches are off. In this case, one of the primary diodes, D_{1OFF}, and all secondary diodes will be forward biased, while the other primary diode, D_{1ON} will be reverse biased. The current that comes out only from the secondary inductor will be received by the load. Alternating between the two mechanisms also applies to other switches.

In mode 5 (when all the switches are OFF), the voltage across the inductors L_p, L_1, L_2, L_3, L_4, and the capacitor C current can be expressed respectively as in (11) to (16). So that the state space mode 5 will be obtained as in (17).

$$\frac{d}{dt}\begin{bmatrix} i_{LP} \\ i_{L1} \\ i_{L2} \\ i_{L3} \\ i_{L4} \\ V_C \end{bmatrix} = \begin{bmatrix} -\frac{R}{L_p} & 0 & 0 & 0 & 0 & -\frac{1}{L_p} \\ 0 & -\frac{R}{L_1} & -\frac{R}{L_1} & -\frac{R}{L_1} & -\frac{R}{L_1} & 0 \\ 0 & -\frac{R}{L_2} & -\frac{R}{L_2} & -\frac{R}{L_2} & -\frac{R}{L_2} & 0 \\ 0 & -\frac{R}{L_3} & -\frac{R}{L_3} & -\frac{R}{L_3} & -\frac{R}{L_3} & 0 \\ 0 & -\frac{R}{L_4} & -\frac{R}{L_4} & -\frac{R}{L_4} & -\frac{R}{L_4} & 0 \\ \frac{1}{C} & -\frac{1}{0} & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{LP} \\ i_{L1} \\ i_{L2} \\ i_{L3} \\ i_{L4} \\ V_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} E_d \tag{17}$$

III. Small-signal Model Analysis

If we wish to construct a converter's control system, we must model the behavior of dynamic converters. However, understanding the dynamic behavior of converters is frequently hampered by the switching and pulse width modulation processes' nonlinear time-varying character. State-space averaging is one of the contemporary control theories that is frequently used to model converters. The state-space averaging method is used to discuss the small-signal model analysis of the proposed converter, which is utilized to approximate the behavior of electronic circuits. A complete converter model including steady-state and dynamic quantities is provided by the state-space averaging technique.

To create an average model of the system, these descriptions are then averaged with respect to how long the duration of the switching process is. The resulting averaged model is non-linear, hence this model should be linearized at the operational point to provide a small signal model, then transformed into an s-domain, which offers transfer functions for the dynamics of the power stage. The analysis starts from the state space equation when the transistor is on and off which is then linearized. The ON condition is stated by d from full working time and the OFF condition is stated by 1/4(1-4d). In CCM, the state-space equations of the proposed converter alternately are shown in (18) and (19).

$$\dot{X} = A_{ON}X + B_{ON}Y \tag{18}$$

$$\dot{X} = A_{OFF}X + B_{OFF}Y \tag{19}$$

i_{LP}, i_o, and V_C are expressed by X as the state space variables and the input variables such as input voltage (E_d) is expressed by Y. A_{ON} and B_{ON} are state space matrix when transistor is ON, and A_{OFF} and B_{OFF} are state space matrix when transistor is OFF.

Since the transistor ON and OFF times are represented by d and 1/4(1-4d), then (18) and (19) can be averaged by the conduction ratio to give (20).

$$\begin{aligned} \dot{X} = &\left[dA_{ON} + \frac{1}{4}(1-4d)A_{OFF}\right]X + \\ &\left[dB_{ON} + \frac{1}{4}(1-4d)B_{OFF}\right]Y \end{aligned} \tag{20}$$

The state space equation of the converter will be obtained as in (21) if (20) is applied to Fig. 2, where R represents the load of the converter.

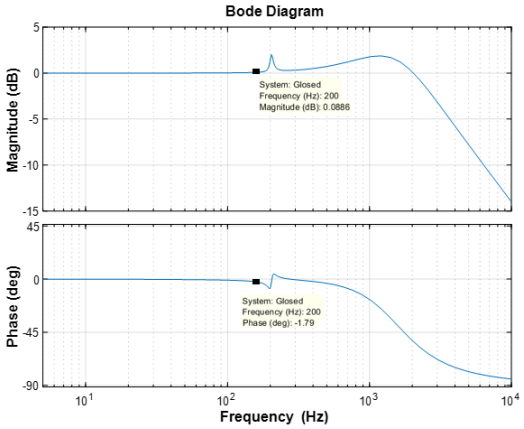

Fig. 8. Bode plot diagram of open-loop system.

To linearize (21), we need to assume that there is a small signal variation in the duty cycle α. So, the duty cycle equation can be written in (22), where the average and small-signal components are represented by the line and tilde above the variable. Eq. (22) can be put in place of (21), giving us (23), with $\frac{1}{L_T} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3} + \frac{1}{L_4}$. And as seen in, the converter's small-signal equation can be produced (24).

$$d\begin{bmatrix} i_{LP} \\ i_o \\ V_C \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_p} \\ 0 & -R(\frac{1}{L_1}+\frac{1}{L_2}+\frac{1}{L_3}+\frac{1}{L_4}) & (\frac{1}{L_1}+\frac{1}{L_2}+\frac{1}{L_3}+\frac{1}{L_4})\alpha \\ \frac{1}{C} & -\frac{\alpha}{C} & 0 \end{bmatrix}\begin{bmatrix} i_{LP} \\ i_o \\ V_C \end{bmatrix} + \begin{bmatrix} \frac{4\alpha}{L_p} \\ 0 \\ 0 \end{bmatrix} E_d \quad (21)$$

$$\alpha = \bar{\alpha} + \tilde{\alpha} \quad (22)$$

By using the Laplace transformation, the converter output current's open-loop transfer function with respect to the duty cycle will be found to be as (25). The open-loop system's bode plot can be shown in Fig. 8 if a plot is created based on the substitution of the parameters in Table 2 to (25). From the small-signal modeling process carried out and based on the resulting graph, it is concluded that the small-signal modeling has made the converter capable of producing an output voltage that matches the given duty cycle. It shows the gain of the i_o versus α remains unity up to 200 Hz, despite there is a minor phase shift at 200 Hz (1.79^o).

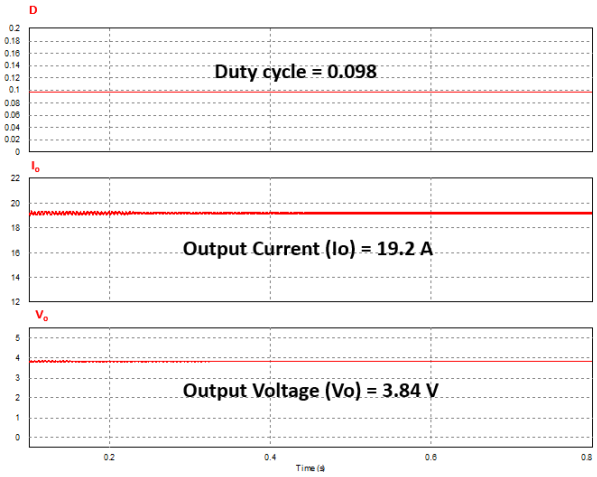

Fig. 9. Simulation result at duty cycle 0.098.

IV. Results and Discussion

PSIM 9.1.4 is used to simulate the open-loop transfer function and evaluate the theoretical analysis of the proposed converter's small-signal model. Simulation is carried out using several parameters as shown in Table 2.

Table 2. Converter Design Parameters

Parameter	Value
E_d	100 Volt
L_1	1.03 mH
L_2	1.03 mH
L_3	1.03 mH
L_4	1.03 mH
L_p	2.6 mH
C	4.7 μF
R	0.2 Ohm

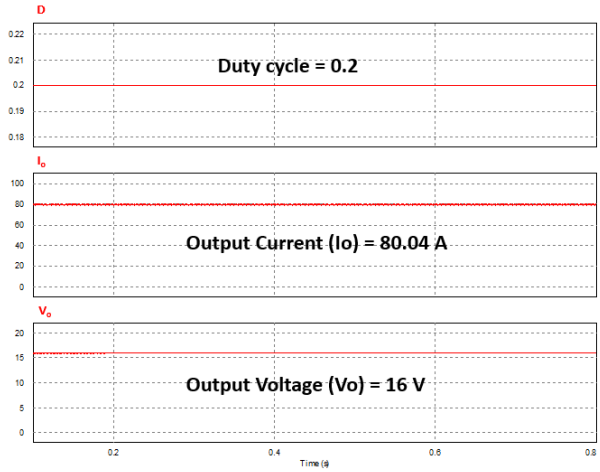

Fig. 10. Simulation result at duty cycle 0.2.

A. Case I, Duty Cycle is at Certain Value

In this case, the results depicted in Fig. 9 and Fig. 10 simulate the impact of a specific duty cycle value. When the duty cycle is set to 0.098, the simulation result is shown in Fig. 9. It is clear that the open-loop system's output voltage and current are, respectively, 19.2 Amperes and 3.84 Volts. Simulation at different values is shown in Fig. 10, where the figure shows the simulation results when the duty cycle is 0.2. As can be observed, the open-loop system's output current and voltage are 80.04 Amperes and 16 Volts, respectively. From these simulations, it can be concluded that the results obtained are in accordance with the theory. In addition, it can also be seen that the proposed converter is capable of producing low output voltage (6 to 26 times lower than the input voltage) and large output current (more than 15 Ampere).

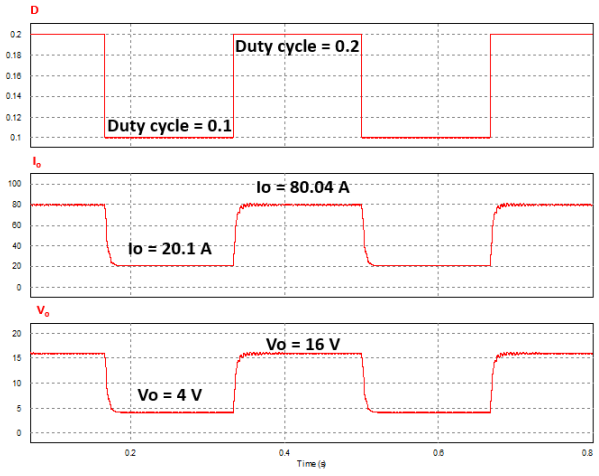

Fig. 11. Simulation result for duty cycle variation.

B. Case II, Duty Cycle Variation (The Duty Cycle Changes Suddenly)

The simulation result of the influence of duty cycle modifications is displayed in Fig. 11. At specific times (t = 0.166 s, 0.33 s, 0.5 s, and 0.66 s), the duty cycle is abruptly changed from 0.1 to 0.2 and vice versa. From the simulation, it is clear that when the duty cycle abruptly changes, the open loop system will do the same, as evidenced by the output current and voltage generated. This outcome supports the notion that the proposed converter's dynamic model is accurate.

V. CONCLUSION

This research proposes a modified DC-DC buck converter open loop system analysis. The investigation of the power converter's working mode and small-signal modeling is presented in this paper. From the research that has been done, it is found that the proposed converter has many advantages, namely the ability to have a high voltage drop ratio and the ability to produce a large output current. A dynamic model of a simplified cascade multiphase DC-DC buck power converter as one of the non-linear converter types has also been found using small-signal modeling. And it is concluded that the small signal modeling that has been done, is able to make the converter produces an output voltage that matches the given duty cycle. Simulations have also been carried out and according to the relationship between the duty cycle and the output current discovered through the analysis of small-signal modeling, it was discovered that the proposed converter had functioned well.

$$\frac{d}{dt}\begin{bmatrix} \overline{i_{LP}}+\widetilde{i_{LP}} \\ \overline{i_o}+\widetilde{i_o} \\ \overline{V_C}+\widetilde{V_C} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_p} \\ 0 & -\frac{R}{L_T} & \left(\frac{\bar{\alpha}+\tilde{\alpha}}{L_T}\right) \\ \frac{1}{C} & -\left(\frac{\bar{\alpha}+\tilde{\alpha}}{C}\right) & 0 \end{bmatrix} \begin{bmatrix} \overline{i_{LP}}+\widetilde{i_{LP}} \\ \overline{i_o}+\widetilde{i_o} \\ \overline{V_C}+\widetilde{V_C} \end{bmatrix} + \begin{bmatrix} \frac{4\bar{\alpha}+4\tilde{\alpha}}{L_p} \\ 0 \\ 0 \end{bmatrix} E_d \tag{23}$$

$$\frac{d}{dt}\begin{bmatrix} \widetilde{i_{LP}} \\ \widetilde{i_o} \\ \widetilde{V_C} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_p} \\ 0 & -\frac{R}{L_T} & \frac{\bar{\alpha}}{L_T} \\ \frac{1}{C} & -\frac{\bar{\alpha}}{C} & 0 \end{bmatrix} \begin{bmatrix} \widetilde{i_{LP}} \\ \widetilde{i_o} \\ \widetilde{V_C} \end{bmatrix} + \begin{bmatrix} \frac{4E_d}{L_p} \\ \frac{V_C}{L_T} \\ -\frac{i_o}{C} \end{bmatrix} \tilde{\alpha} \tag{24}$$

$$\frac{\widetilde{i_o}(s)}{\widetilde{\alpha}(s)} = \frac{L_pCV_Cs^2 - L_pi_o\bar{\alpha}s + 4\bar{\alpha}E_d + V_C}{L_pL_TCs^3 + L_pCRs^2 + (L_T + L_p\bar{\alpha}^2)s + 1} \tag{25}$$

ACKNOWLEDGEMENT

This research has been fully supported by The Institution of Research and Community Services (LPPM) University of Surabaya.

REFERENCES

[1] Z. Tang, Y. Yang, and F. Blaabjerg, "Power electronics: The enabling technology for renewable energy integration," *Csee Journal of Power and Energy Systems*, vol. 8, no. 1, pp. 39–52, 2022. Doi: 10.17775/Cseejpes.2021.02850.

[2] S. Hasanpour, A. Baghramian, and H. Mojallali, "Analysis and modeling of a new coupled-inductor buck-boost DC-DC converter for renewable energy applications," *IEEE Transactions On Power Electronics*, vol. 35, no. 8, pp. 8088–8101, 2020. Doi: 10.1109/Tpel.2019.2962325.

[3] H. S. Lee, and J. J. Yun, "High-efficiency bidirectional buck-boost converter for photovoltaic and energy storage systems in a smart grid," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4316–4328, 2019. Doi: 10.1109/Tpel.2018.2860059.

[4] S. Lu, K. Sun, H. Shi, Y. Li, and G. Cao, "Evaluation of high step-up power conversion systems for large-capacity photovoltaic generation integrated into medium voltage DC grids," *Chinese Journal Of Electrical Engineering*, vol. 7, no. 4, pp. 3–14, 2021. Doi: 10.23919/Cjee.2021.000033.

[5] Z. Fang, Z. Wei, Z. Huang, and F. Liu, "Onboard energy storage system based on interleaved high-conversion-ratio quasi-resonant converter with small characteristic impedance," *IEEE Transactions on Vehicular Technology*, vol. 70, no. 5, pp. 4238–4251, 2021. Doi: 10.1109/Tvt.2021.3071525.

[6] S. S. Varghese and S. George, "Analysis of AC-DC converter based on power factor and THD," *International Journal Emerging Technology and Advance Engineering*, vol. 3, pp. 350–356, 2013.

[7] M. K. Kazimierczuk, Pulse-width modulated DC-DC power converters, Second Edition, 2015.

[8] M. Amiri and H. Farzanehfard, "A high-efficiency interleaved ultra-high step-down DC-DC converter with very low output current ripple," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 7, pp. 5177–5185, 2019. Doi: 10.1109/Tie.2018.2869348.

[9] O. Kirshenboim and M. M. Peretz, "High-efficiency nonisolated converter with very high step-down conversion ratio," *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 3683–3690, 2017. Doi: 10.1109/Tpel.2016.2589321.

[10] M. Esteki, B. Poorali, E. Adib, and H. Farzanehfard, "Interleaved buck converter with continuous input current, extremely low output current ripple, low switching losses, and improved step-down conversion ratio," *IEEE Transactions On*

Industrial Electronics, vol. 62, no. 8, pp. 4769–4776, 2015. Doi: 10.1109/Tie.2015.2397881.

[11] W. Hassan, J. L. Soon, D. Dah-Chuan Lu, and W. Xiao, "A high conversion ratio and high-efficiency bidirectional DC-DC converter with reduced voltage stress," *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 11827–11842, 2020. Doi: 10.1109/Tpel.2020.2987083.

[12] Y. Guan, C. Cecati, J. M. Alonso, and Z. Zhang, "Review of high-frequency high-voltage-conversion-ratio DC–DC converters," *IEEE Journal of Emerging And Selected Topics in Industrial Electronics*, vol. 2, no. 4, pp. 374–389, 2021. Doi: 10.1109/Jestie.2021.3051554.

[13] G. H. De Alcantara Bastos, L. F. Costa, F. L. Tofoli, G. V. T. Bascope, and R. P. T. Bascope, "Nonisolated DC-DC converters with wide conversion range for high-power applications," *IEEE Journal Of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 749–760, 2020. Doi: 10.1109/Jestpe.2019.2892977.

[14] S. Marconi, G. Spiazzi, A. Bevilacqua, and M. Galvano, "A novel integrated step-up hybrid converter with wide conversion ratio," *IEEE Transactions on Power Electronics*, vol. 35, no. 3, pp. 2764–2775, 2020. Doi: 10.1109/Tpel.2019.2931875.

[15] C. G. Zogogianni, E. C. Tatakis, and M. S. Vekic, "Non-isolated reduced redundant power processing DC/DC converters: A systematic study of topologies with wide voltage ratio for high-power applications," *IEEE Transactions on Power Electronics*, vol. 34, no. 9, pp. 8491–8502, 2019. Doi: 10.1109/Tpel.2018.2889294.

[16] N. Elsayad, H. Moradisizkoohi, and O. A. Mohammed, "Design and implementation of a new transformerless bidirectional DC-DC converter with wide conversion ratios," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 9, pp. 7067–7077, 2019. Doi: 10.1109/Tie.2018.2878126.

[17] A. B. Ganesen, N. Prameswari, F. K. Nuraziz, J. Furqani, A. Rizqiawan, and P. A. Dahono, "Simplified cascade multiphase DC-DC buck power converter for low voltage large current applications: Part I-steady-state analysis," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol. 12, no. 3, 2021. Doi: 10.11591/Ijpeds.V12.I3.Ppxx-Yy.

[18] P. A. Dahono, "Simplified cascade Mmltiphase DC-DC boost power converters for high voltage-gain and low-ripple applications," *International Journal of Power Electronics and Drive Systems*, vol. 12, no. 1, pp. 273–285, 2021. Doi: 10.11591/Ijpeds.V12.I1.Pp273-285.

[19] I. Erdin, R. Achar, and K. Erdin, "Power integrity aware approach to dynamic analysis of buck converters," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 8, no. 1, pp. 32–40, 2018. Doi: 10.1109/Tcpmt.2017.2741967.

[20] J. Mahdavi, A. Emaadi, M. D. Bellar, and M. Ehsani, "Analysis of power electronic converters using the generalized state-space averaging approach," *IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications*, vol. 44, no. 8, pp. 767–770, 1997.

[21] K. Natarajan and M. Yektaii, "Modeling of DC-DC buck converters for large-signal frequency response and limit cycles," *IEEE Transactions on Circuits and Systems Ii: Express Briefs*, vol. 53, no. 8, pp. 712–716, 2006. Doi: 10.1109/Tcsii.2006.876380.

[22] X. Li, X. Ruan, Q. Jin, M. Sha, and C. K. Tse, "Small-signal models with extended frequency range for DC-DC converters with large modulation ripple amplitude," *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 8151–8163, 2018. Doi: 10.1109/Tpel.2017.2773641.

[23] A. Chadha and M. K. Kazimierczuk, "Small-signal modeling of open-loop PWM tapped-inductor buck DC-DC converter in CCM," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 7, pp. 5765–5775, 2021. Doi: 10.1109/Tie.2020.2996157.

[24] M. T. Iqbal and A. I. Maswood, "An explicit discrete-time large and small-signal modeling of the dual active bridge DC–DC converter based on the time scale methodology," *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 2, no. 4, pp. 545–555, 2021. Doi: 10.1109/Jestie.2021.3087942.

[25] Z. Zhang, S. Tian, and K. D. T. Ngo, "Small-signal equivalent circuit model of quasi-square-wave flyback converter," *IEEE Transactions on Power Electronics*, vol. 32, no. 8, pp. 5885–5888, 2017. Doi: 10.1109/Tpel.2017.2661320.